

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

- 1 1. (Currently Amended) A Booth encoding circuit comprising:
 - 2 a plurality of cells, wherein at least one of said cells
 - 3 comprises:
 - 4 a plurality of inputs;
 - 5 a first plurality of transistors forming a ~~first~~ NAND logic
 - 6 stage, wherein at least one of said inputs is connected to at
 - 7 least one of said first plurality of transistors;
 - 8 a second plurality of transistors forming a ~~second~~ an OR
 - 9 logic stage, wherein at least one of said inputs is connected to
 - 10 at least one of said second plurality of transistors;
 - 11 a first output inverter connected to at least one of said
 - 12 second plurality of transistors;
 - 13 a first switching means connected to at least one of said
 - 14 first plurality of transistors;
 - 15 a second switching means connected to said first output
 - 16 inverter;
 - 17 a second output inverter connected to said first switching
 - 18 means and said second switching means, wherein within a critical
 - 19 path of said Booth encoding circuit said first output inverter
 - 20 drives said second output inverter.
- 1 2. (Original) The Booth encoding circuit of claim 1, wherein
- 2 within said critical path of said Booth encoding circuit said
- 3 first output inverter drives said second output inverter via said
- 4 second switching means.
- 1 3. (Original) The Booth encoding circuit of claim 2, wherein
- 2 said first switching means comprises a first transfer gate switch

3 and said second switching means comprise a second transfer gate
4 switch.

4. (Canceled)

1 5. (Currently Amended) The Booth encoding circuit of claim 4 1,
2 wherein said critical path comprises at least two of said second
3 transistors, said first output inverter, said second switching
4 means, and said second output inverter.

1 6. (Original) The Booth encoding circuit of claim 5, wherein a
2 critical path transistor level within said cell is less than six
3 and a critical path transistor level within said Booth encoding
4 circuit is less than ten.

1 7. (Currently Amended) The Booth encoding circuit of claim 4 1,
2 wherein an output of said second output inverter is logically
3 expressed by the formula $Y_{2n+1} * (Y_{2n} * Y_{2n-1}) + Y_{2n+1} * (Y_{2n} + Y_{2n-1})$,
4 wherein said plurality of inputs comprise Y_{2n} , Y_{2n-1} , and Y_{2n+1} .

1 8. (Original) The Booth encoder of claim 2, wherein said cell
2 further comprises an input inverter connected to said first
3 switching means and at least one of said inputs.

1 9. (Original) The Booth encoder of claim 8, wherein at least
2 one of said inputs is connected to said second switching means.

1 10. (Currently Amended) A multiplier comprising:
2 A Booth encoding circuit, wherein said Booth encoding
3 circuit comprises a plurality of cells, wherein at least one of
4 said cells comprises:
5 a plurality of inputs;

6 a first plurality of transistors forming a ~~first~~ NAND logic
7 stage, wherein at least one of said inputs is connected to at
8 least one of said first plurality of transistors;

9 a second plurality of transistors forming a ~~second~~ an OR
10 logic stage, wherein at least one of said inputs is connected to
11 at least one of said second plurality of transistors;

12 a first output inverter connected to at least one of said
13 second plurality of transistors;

14 a first switching means connected to at least one of said
15 first plurality of transistors;

16 a second switching means connected to said first output
17 inverter;

18 a second output inverter connected to said first switching
19 means and said second switching means, wherein within a critical
20 path of said Booth encoding circuit said first output inverter
21 drives said second output inverter.

1 11. (Original) The multiplier of claim 10, wherein within said
2 critical path of said Booth encoding circuit said first output
3 inverter drives said second output inverter via said second
4 switching means.

1 12. (Original) The multiplier of claim 11, wherein said first
2 switching means comprises a first transfer gate switch and said
3 second switching means comprise a second transfer gate switch.

13. (Canceled)

1 14. (Currently Amended) The multiplier of claim ~~13~~ 10, wherein
2 said critical path comprises at least two of said second
3 transistors, said first output inverter, said second switching
4 means, and said second output inverter.

1 15. (Original) The multiplier of claim 14, wherein a critical
2 path transistor level within said cell is less than six and a
3 critical path transistor level within said Booth encoding circuit
4 is less than ten.

1 16. (Currently Amended) The multiplier of claim ~~13~~ 10, wherein
2 an output of said second output inverter is logically expressed
3 by the formula $Y_{2n+1} * (Y_{2n} * Y_{2n-1}) + Y_{2n+1} * (Y_{2n} + Y_{2n-1})$, wherein
4 said plurality of inputs comprise Y_{2n} , Y_{2n-1} , and Y_{2n+1} .

1 17. (Original) The Booth encoder of claim 11, wherein said cell
2 further comprises an input inverter connected to said first
3 switching means and at least one of said inputs.

1 18. (Original) The Booth encoder of claim 17, wherein at least
2 one of said inputs is connected to said second switching means.

1 19. (Currently Amended) A multiply-accumulate module comprising:
2 a multiplier, wherein said multiplier comprises:
3 A Booth encoding circuit, wherein said Booth encoding
4 circuit comprises a plurality of cells, wherein at least one of
5 said cells comprises:
6 a plurality of inputs;
7 a first plurality of transistors forming a ~~first~~ NAND logic
8 stage, wherein at least one of said inputs is connected to at
9 least one of said first plurality of transistors;
10 a second plurality of transistors forming a ~~a-second~~ an OR
11 logic stage, wherein at least one of said inputs is connected to
12 at least one of said second plurality of transistors;
13 a first output inverter connected to at least one of said
14 second plurality of transistors;

15 a first switching means connected to at least one of said
16 first plurality of transistors;
17 a second switching means connected to said first output
18 inverter;
19 a second output inverter connected to said first switching
20 means and said second switching means, wherein within a critical
21 path of said Booth encoding circuit said first output inverter
22 drives said second output inverter.

1 20. (Original) The multiply-accumulate module of claim 19,
2 wherein a critical path transistor level within said cell is less
3 than six and a critical path transistor level within said Booth
4 encoding circuit is less than ten.